and fix flaws during the design stage can then directly be used as the test-bench during test and verification stages.

Using Simulink for Model-based design, an engineer can utilise multiple data-types and perform multi-rate simulations. The effects of changing design parameters are easily determined due to the fast simulation speeds. In this example, the designer can choose to modify the frequency error introduced by the transmission channel, and study its effect on the bit-error rate.

Advanced blocksets such as the Signal Processing Blockset and Communications Blockset also provide the additional functionality needed to create and maintain comprehensive and complete system specifications that can double as high-performance test benches for hardware verification. Additionally, model coverage and test coverage can now be included and quantified at the system level.

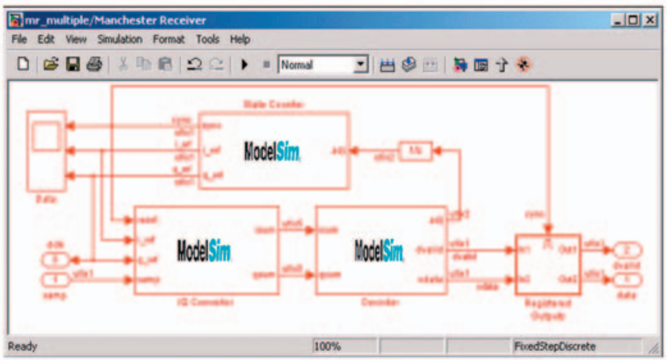
Another major boost to the speed and efficiency of hardware verification comes from using multiple HDL simulators in one integrated simulation. An engineer can perform distributed hardware verification by incorporating multiple HDL entities, simultaneously executing on multiple RTL simulators on multiple machines into a single system-level test-bench. This too is not a novel idea.

However, until recently, there was no easy way to synchronise these various HDL entities. Nor could one ensure that the HDL entities receive accurate data of the right data types at correct intervals during the simulation.

For Model-based design, new co-simulation interfaces provide this support as well, between the system-level simulator and the RTL simulator, to facilitate distributed verification that is user-transparent and efficient.

Figure 5 shows the simple example of three VHDL entities, connected through Simulink, which could possibly execute in multiple ModelSim sessions on separate machines by using a single Link for ModelSim co-simulation interface.

Fig 5: Three VHDL entities connected through Simulink



Hardware verification is the most time-consuming task in the hardware design process, and important advances are being made to face this challenge by approaching it from several directions simultaneously. Advances in simulators and co-simulation interfaces now provide engineers with several major improvements in functional hardware verification.

Model-based design is proving to be so attractive to engineers that a variety of vendors are introducing products and technologies to help hardware engineers implement, optimise, and verify signal processing applications on FPGAs and ASICs.

This trend is expected to significantly grow and expand in the near future. In addition, Model-based design will expand to include and support more advanced verification needs such as assertion-based and formal verification of hardware at the system level.

Arun Mulpur is with The MathWorks

Esterel Technologies introduces version 5.1 of SCADE

SCADE 5.1 from Esterel Technologies provides a seamless path from formal software specification to safe embeddable production C code. This version adds a Model Test Coverage module which allows the measurement of the coverage of a SCADE model by a high-level requirements-based test suite.

The purpose of the analysis is to assess how thoroughly the behavior of a SCADE model has been explored by simulation. A primary objective of MTC is to detect unintended functions. MTC methodology has been designed with the cooperation of several major industrial actors like Airbus and Eurocopter. MTC will be DO-178B qualified as a verification tool.

MTC plays an integral part in the SCADE Combined Testing Process methodology that enables a seamless verification process from the high level requirements of a system to the object code of the software running on the hardware target.

The Combined Testing process includes in particular the Compiler Verification Kit. CVK is a package of SCADE models and tests that enable the testing of all SCADE functionality for a selected cross-development tool chain and a microprocessor. It enables the verification of a SCADE deployment platform and proves that SCADE-generated code will execute correctly on a given target platform. The SCADE CVK needs to be executed only once for any cross-compiler/ target microprocessor platform.

For safely managing multi-users projects a Model Diff function of the SCADE Editor allows project team to pinpoint semantic differences between two versions of a model, and then to locate precisely the differences including in the graphics.

The SCADE Design Verifier technology enables software designers to detect crucial bugs early in the development process and accurately. Because it is a recognized fact that the 'Division by Zero' bug is one of the most common bugs in real-time embedded software developments, Design Verifier 5.1 incorporates a ready-to-use Check Division-by-Zero function that reports on actual divisions-by-zero.

The Operating mode means that as a SCADE model is being designed a Check Division-by-Zero function can be called at anytime. In seconds, counter-examples are provided, then the model is tuned by adding precise protection to the variables that are pointed out at risk only. The operation can be redone as long as a report is provided that falsifies the formal Check Division-by-Zero proof objective. When the Design Verifier doesn't detect any error, the process is completed.

SCADE 5.1 supports two new strategic partnerships to create the first Certified Software Factory with the SCADE Gateway to I-LOGIX Rhapsody and the connection of SCADE with Green Hills' INTEGRITY RTOS and Compilers.

The SCADE Gateway to Rhapsody intends to combine the respective strengths of UML and SCADE to develop safety-critical systems. By using UML to specify the system's high-level requirements and architecture, and then SCADE to formally specify the software behavior, an efficient seamless flow is provided from the initial requirement analysis phase down to the final integration on the target platform.

SCADE Qualified Code Generator (KCG) will also produce code that will be automatically integrated with Green Hills Software's INTEGRITY-178B Level A and IEC61508 certified INTEGRITY RTOS's. Furthermore, Green Hills Software's industry leading compilers will be pre-qualified through SCADE's Compiler Verification Kit (CVK) ensuring that any code produced by SCADE and then compiled by Green Hills Software's compilers.