

space and cost savings. This, again, could prove an attractive option in value-based applications.

Actel has assembled a full suite of tools for the development of designs with CoreMP7. Key amongst these is CoreConsole, a block stitcher and IP deployment platform (IDP). This new tool provides an intuitive and easy-to-use graphical user interface that facilitates rapid implementation of other IP blocks and a subsystem around the processor.

Consisting of two components – the IDP tool itself and an IP vault – CoreConsole supports the integration of functions such as timers and UARTs with Actel DirectCores delivered in the IP Vault, as well as third-party and user-defined IP blocks.

CoreConsole allows users to reduce system development time and perform system-level evaluation. Subsystem peripherals – including an AHB bus interface, APB bus interface, AHB-to-APB bridge, memory controller, interrupt controller, timers, serial interfaces and buffered I/O – are delivered as configurable RTL code as part of the IDP.

By working at the design entry phase of the design process and dealing mainly with RTL, CoreConsole integrates easily with Actel's existing Libero IDE and other tools. As well as enabling users to configure IP blocks for use in their application, it also generates a system interconnect testbench that can be used to debug and validate the implementation of the final application within the FPGA fabric.

The tool can also output drivers and other files to other software development tools to enable faster development of the programs that run on the core itself: these can be built, debugged and managed via a version of the ARM RealView Developer Kit designed specifically for use with CoreMP7.

By combining a secure, cost-effective, low-power and configurable FPGA platform with the market's undisputed leader in processor cores, ARM and Actel have made it practical to implement 32-bit processing even in the most cost-sensitive embedded applications.

QuickLogic embeds SDIO interfaces in to FPGAs

QuickLogic has released intellectual property for an SDIO Host Controller core that can be embedded into its Eclipse II 'microwatt' FPGAs. Reference designs based on QL8150 and 8325 Eclipse II FPGAs - devices with 188,000 and 320,000 gates - are available to shorten development cycles.

The SDIO reference design provides a complete bridging/controlling solution for interfacing Intel PXA27x embedded processors with SDIO peripherals and/or SD memory. The inherent benefits of Eclipse II based solutions include a small footprint, ultra low power consumption, and proven high performance. These attributes are critical for products such as portable global positioning systems, smart phones, portable media players, and portable industrial systems.

The SDIO intellectual property, embedded in the reference design, can be operated at a clock frequency of up to 52MHz, exceeding the SDIO specification of 25MHz. The programmability of the SDIO-enabled reference design allows designers to incorporate their unique logic requirements and tune for power or performance depending on product specifications.

The company has demon-

strated that its SDIO reference design can deliver improvements in the read/write performance of SD memory cards. Using the company's Mobile Applications Board (MAB), the gains achievable were up to three times the performance versus the PXA27x processor's native mode at the same frequency, and up to five times the performance at higher frequencies.

The SDIO reference design can be combined with further IP to support designs that implement multiple interfaces to the Intel PXA27x, allowing designers to add peripheral functions such as 802.11g and USB using a single FPGA device.

The SDIO IP and reference design provides designers with an easy-to-implement and proven SDIO bridging/controlling solution. The reference design includes a QuickLogic MAB, a QuickLogic QL8325 Eclipse II 'microwatt' FPGA, and a Microsoft Windows CE driver compatible with the Intel PXA27x processor 'Mainstone' II DVK. The reference design has been hardware and software proven with a Kingston 1 Gbyte SD memory card, and SanDisk 64Mbyte SD memory card.

QuickLogic's MAB for the Intel PXA27x-based Processor Developer's Kit provides seam-

less connectivity between the Intel XScale processor and peripheral interfaces such as Mini PCI, CardBus, SDIO and IDE.

The daughtercard enables IP development and performance verifications for these interfaces. It connects into the VLIO connector of the DVK, which allows designers to make system measurements and architecture tradeoffs including power consumption, performance and cost.

Complete solution packs are available for both Wi-Fi and HDD connectivity. They include the MAB, Eclipse II QL8325 device in the 484-ball BGA package, reference design files and software drivers for Windows CE, Windows Mobile, and Linux. It provides support for IDE, Mini PCI, PCI, Card Bus, or SDIO depending upon configuration.

QuickLogic says the MAB lets designers begin software development prior to receiving final hardware. This ability to design hardware and software in parallel can provide a critical competitive advantage by significantly reducing time spent in development of popular portable products including global positioning systems (GPS), smart phones, portable media players, and portable industrial systems.

Quicklogic SDIO host controller core

