

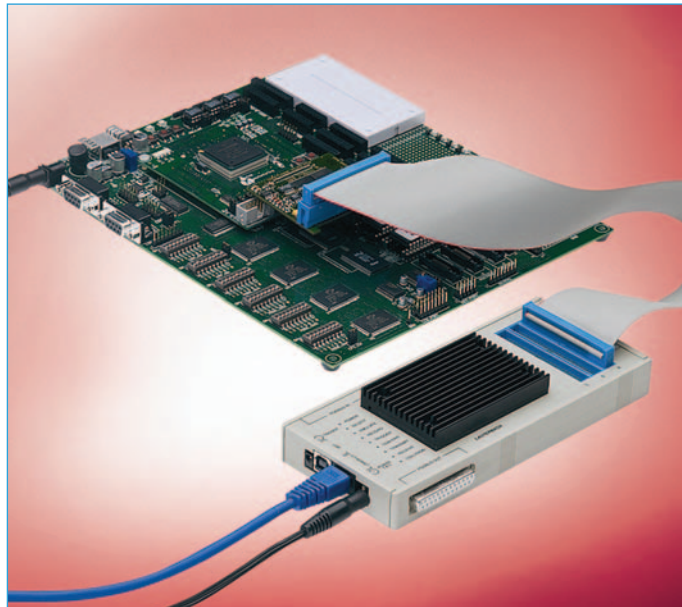
Lauterbach support for TI and Altera

Lauterbach's TRACE32 ICD and TRACE32 PowerTools debuggers now support the Texas Instruments TMS320C6000 family of processors. The TRACE32 ICD and PowerDebug modules, which can be connected to the host computer over a parallel port, USB or Ethernet, allow fast access to all internal chip units, such as on-chip hardware breakpoints, peripheral equipment, registers, EEPROM, and flash memory, over the processor's JTAG interface.

An unlimited number of software breakpoints in the RAM and flash memories, debugging at HLL and assembler levels, programmable flash memory, and support of the most widely used C and C++ compilers are all provided.

Real-time tracing is being developed. The trace memory can record 128megaframes and operates at a maximum rate of 300MHz. Each recording is given a time stamp with a resolution of 10ns. In this way, code coverage and performance analysis can be performed, and time diagrams and statistics can be generated.

Graphical views enable error



detection in common DSP or imaging applications. Multicore debugging supports the debugging of heterogeneous systems (for example, together with an ARM or MIPS core).

The debuggers currently support the TMS320C62x 32bit Fixed Point 1200-2400 MIPS, TMS320C64x 32bit Fixed Point 2400-8000 MIPS, TMS320C67x 32bit Floating Point, 600MFLOPS - 1250MFLOPS.

Lauterbach are also providing multi-processor debug support for Altera's Nios II software embedded processor. Software engineers can now take advantage of a robust software environment tailored to debugging multiple Nios II processors in an Altera FPGA or HardCopy series structured ASIC. By implementing multiple soft-core processors in a single FPGA, system designers can achieve a

high level of performance with the flexibility to adapt to a dynamic design environment.

The Lauterbach multi-processor debug solution enables the display and control of multiple Nios II processors in the FPGA. Each Nios II processor can be logically grouped and synchronized, responding to start, step, and break commands simultaneously. Additionally, cross-breakpoint awareness enables a user to halt the system when a set of processors have all reached their assigned breakpoints.

The solution relies on Lauterbach's TRACE32-PowerView debugger software to provide a unified, graphical environment for debugging one or more Nios II processors. Meanwhile, Lauterbach's TRACE32-PowerDebug hardware debug module gives designers a simple hardware connection to their system, operating over a single JTAG connection to the Altera device.

External, time-stamped trace capture is also provided over a high-speed Mictor connector to the Nios II system, providing users 512Mbytes of capture depth at 300MHz.

Phyton emulator integrates with Keil IDE

Phyton has integrated its PICE-52 emulator within the Keil μ Vision Debugger. Phyton's PICE-52 emulator has traditionally supported both source-level debugging and project-level development for the Keil 8051 C compiler.

The company says many developers who use PICE-52 in combination with the Keil μ Vision IDE have requested that the μ Vision Debugger drive PICE-52 directly. After several months of close collaboration between developers from Phyton and Keil, this has now been implemented.

μ Vision does not replace Phyton's own IDE but provides additional options for controlling PICE-52.

While most of the basic func-

tions of PICE-52 are supported right from μ Vision, some features such as trace, memory coverage, and complex breakpoints, are not yet accessible for observation and control. Phyton plans to include these features in the integrated system in the future.

Keil Software is also providing μ Vision3 support for the Infineon XC800 8-bit microcontroller series. The PK51 Professional Developers Kit and the μ Vision3 IDE/debugger integrate compiler, assembler, editor, project manager, debugger, and CPU and peripheral simulator in a single intelligent environment (the same environment is used for the Infineon C500, C16x, and XC16x series).

The Infineon XC866 is the first product of the advanced 8-bit XC800 microcontroller family, which combines the extended performance of a high-speed 8051 core with powerful on-chip peripherals and Flash memory. System costs are minimized through high integration, on-chip oscillator, and 3.3V or 5.0V single supply voltage. Key features of the XC866 are the CAPCOM6E unit, which provides flexible PWM generation, and a new 10-bit A/D Converter, with extended functionality like comparator mode. An enhanced UART supports LIN-wake-up-message.

μ Vision now includes complete, cycle-accurate simulation for the XC800 device family. This is required to test complex

applications like motor control systems. The built-in logic analyzer and performance analyzer in the μ Vision debugger/simulator enable precise timing analysis and, when combined with simulation scripts that provide input signals, provide a complete, safe test environment that requires no interaction with motors or other external hardware.

Single-stepping, which is not possible in live-hardware testing, is possible under simulation. For even higher-fidelity testing, the AGSI interface to μ Vision provides access to external modelling tools like MATLAB/Simulink which provides Software-in-the-Loop (SiL) analysis of control algorithms.