

Company	This DSP family is: (1)	It is available as:	Fixed (2)	Word size	Accumulator	Floating (3)	Word size	Accumulator	Architecture	CISC/RISC?	No. of instructions	Implementation type	Number of separate functional units
3DSP	MCU-based	Core	X	32	48				Mod. Harvard	RISC	50	SuperScalar SIMD	four 16-bit multiplier, four 32-bit accumulates, eight 8-bit multiplier, four loads, four memory address calculations, eight 8-bit adds, four 16-bit adds, two 32-bit adds, one 32-bit shift
3DSP	MCU-based	Core	X	32	48				Mod. Harvard	RISC	50	Scalar SIMD	two 16-bit multiplier, two 32-bit accumulates, four 8-bit multiplier, two loads, two memory address calculations, four 8-bit adds, two 16-bit adds, one 32-bit adds, one 32-bit shift
AMSI		Core	X	8 to 32	Up to 64				Mod. Harvard	RISC	20	SuperScalar	one multiply-accumulate, one ALU, two address calculation
Analog Devices	MCU-based	Standard	X	16 bit	40				Mod. Harvard	RISC	70	Scalar	one ALU/MAC/shifter, two memory reads, two address calculation, one instruction fetch
Analog Devices	MCU-based	Standard	X	32	40	X	32 & 40	40	Mod. Harvard	CISC	34	Scalar	ADSP-2106x : one ALU, one multiplier, two address calculations with circular buffering, one cache, two DMA address calculation, three transfers from/to memory, one timer operations, four serial ports accesses, six link port access, four external port DMA ADSP-2116x : two ALU, two Multiplier, four address calculations with circular buffering, one cache, two DMA address calculation, three transfers from/to memory, one timer operation, four serial ports accesses, six link port access, four external port DMA
ARM	MPU-based	Core	X	32	32/64				Harvard	RISC	Similar to ARM instruction set architecture. VSTF	Scalar	Multiply and accumulate in parallel
BOPS	MCU-based	Core	X	8,16,32	40,64	X	32	32	ManArray	RISC	32-bit	iVLIW - Indirect VLIW in a manifold array	1x1 5-32 bit VLIW instructions: 16-bit fixed - two ALU, two multiplier, four address, four load, four store, four DMA ; 32-bit float - one ALU, one DMA 2x2; 16-bit Fixed - eight ALU, eight multiplier, eight address, eight load, eight store, eight DMA, eight intercore; 32-bit float - four ALU, four multiplier, eight address, four load, four store, eight DMA, four intercore 4x4: 16-bit fixed - 32 ALU, 32 Multiplier, 32 Address, 32 load, 32 store, 32 DMA, 32 Intercore; 32-bit float - 16 ALU, 16 multiplier, 16 address, 16 load, 16 store, 16 DMA, 16 intercore
Catalina	n/a	Standard/Core	X	32	36				Dataflow	n/a	18	Vector Processor	25
Hitachi	MCU-based	Standard	X	16 bit	16 bit				Mod. Harvard	RISC	154	Scalar	one ALU, one multiplier, two address
Hitachi	MCU-based	Standard	X	16	16				Mod. Harvard	RISC	154	Scalar	one ALU, one multiplier, two address
Hitachi	MPU-based	Standard	X	16	16				Mod. Harvard	RISC	154	Scalar	one ALU, one multiplier, two address
Hitachi	MPU-based	Standard	X	16	16				Mod. Harvard	RISC	154	Scalar	one ALU, one multiplier, two address
Hitachi	MPU-based	Standard	X	16	16				Mod. Harvard	RISC	156	Scalar	1 ALU, 1 Multiplier, 2 Address
Hitachi	MPU-based	Standard				X	32/64	32/64	Von Neuman	RISC	154	SuperScalar	three ALU, four multiplier, two address
Hitachi	MPU-based	Standard				X	32/64	32/64	Von Neuman	RISC	154	SuperScalar	three ALU, four multiplier, two address
Infineon	MPU-based	Core	X	16	40				Mod. Harvard/Reconfigurable	CISC	90	SuperScalar	18
Infineon	MCU-based	Standard/Core	X	16	48				Von Neuman	RISC	409	SuperScalar	three ALU, two multiplier, one address

Company	This DSP family is: (1)	It is available as:	Fixed (2)	Word size	Accumulator	Floating (3)	Word size	Accumulator	Architecture	CISC/RISC?	No. of instructions	Implementation type	Number of separate functional units
LSI Logic		Standard/Core	X	16	40				Mod. Harvard	RISC	16-bit instruction set	SuperScalar	three ALU, two multiplier, two address
Lucent		Standard	X	16	36				Mod. Harvard	RISC	80	Scalar	one ALU, one multiplier, two address, two post modify
Lucent		Standard/Core	X	16	40				Mod. Harvard	RISC	180	Scalar	two ALU, two multiplier, two address, two post modify
Phillips	MCU- and MPU-based	Core	X	16	16/40				Dual Harvard	CISC	n/a	Modified VLIW through application specific instructions	four ALU, two multiplier, dedicated shift, barrelshift/normaliser, two address calculation, saturation/scaling/rounding
Philips	MCU- and MPU-based	Core	X	24	24/56				Dual Harvard	CISC	n/a	Modified VLIW through application specific instructions	four ALU, two multiplier, dedicated shift, barrelshift/normaliser, two address calculation, saturation/scaling/rounding
Philips	MCU- and MPU-based	Standard	X	8/16/32	64		32	64	Mod Harvard	RISC	210	VLIW	5
Star*Core	MPU-based	Core	X	16	40				Mod Harvard	RISC	185	Variable length execution set (VLES): a multi-issue architecture that allows up to 6 executable 16-bit RISC instructions, and 2 prefix instructions to be issued simultaneously w/no alignment or NOP padding	four DALU (MAC, ALU or BFU), two address
Texas Instruments	More DSP-based	Standard	X	16	32				Mod Harvard	CISC	87		32-bit CALU, three scaling shifters, 16-bit x 16-bit multiplier with 32-bit product capability, 32-bit accumulator
Texas Instruments	DSP-based	Standard	X	16	32				Mod Harvard	CISC	87		32-bit CALU, three scaling shifters, 16-bit x 16-bit multiplier with 32-bit product capability, 32-bit accumulator
Texas Instruments	DSP-based	Standard	X	32	40	X	32	32	Mod Harvard	RISC	50	VLIW	Eight orthogonal functional units including two multipliers and six ALUs
Texas Instruments	DSP-based	Standard	X	32	32	X	40	40	Mod Harvard	RISC	100+	Scalar	two address, two ALUs, one branch
VLSI	MPU-based	Core	X	16	40				Mod Harvard	RISC	35	Scalar	ALU/Multiplier + two address + one loop
VLSI	MPU-based	Core	X	24	56				Mod Harvard	RISC	68	Scalar	ALU/Multiplier +one Address + one loop
ZiLOG	MCU-based	Standard, Core	X	16	24				Mod Harvard	RISC	30 (Clarkspur)	Scalar	one ALU, one multiplier, one address

Company	No. of Gen'l purpose calculation units	Program Memory	Data Memory	Min. Single -Tap FIR Filter Cycle Time	Upward Code Compatible w/ What Other Part Family	C Compiler Available	Assembly Language Optimizations Tools Available	Architectural Support for C Stack Frames	JTAG Support for Emulation	Full JTAG Test Support
3DSP	75	Up to four giga 32-bit words, user can implement with ROM, RAM, FLASH, cache capability is provided in user selectable blocks.	Up to 4 GB user can implement with ROM, RAM, FLASH.	6.4 ns. Note: this uses only one eighth or the processing capability of a single cycle. For example, if eight such operations were required each would average only 0.8 ns.	Yes	Yes	Yes	Yes	Yes	Yes
3DSP	75	Up to four giga 32-bit words, user can implement with ROM, RAM, FLASH, cache capability is provided in user selectable blocks.	Up to 4 GB user can implement with ROM, RAM, FLASH.	6.4 ns. Note: this uses only one eighth or the processing capability of a single cycle. For example, if four such operations were required each would average only 1.6 ns.	Yes	Yes	Yes	Yes	Yes	Yes
AMSI	One (ALU)	32 bit words; Internal, ROM Memory	8- to 32-bit words; internal, RAM memory	10 ns for 16-bit implementation	No	No	No	No	No	No
Analog Devices	ALU, MAC, Shifter, 2x Data Address Generators.	Up to 48K x 24. Internal, Shared, RAM	Up to 56K x 16, internal	13 ns	Code Compatible w/ all 21xx family members	Yes	No	Yes	No	No
Analog Devices	ADSP-2106x: one ALU, one multiplier, two address calculations with circular buffering, two DMA address calculation. ADSP-2116x: two ALU, two multiplier, four address calculations with circular buffering, two DMA address calculation.	Number of memory locations, external: 4 gigawords, Internal: 128 32-bit words, word width (bits) :32-bit, program memory: 512 kbit to 4 Mbits, Shared, RAM		15 ns	2116x is upward code compatible with 2106x	Yes	No	Yes	Yes	Yes
ARM	1	Internal; ROM, RAM, EPROM, EEPROM	Internal, external, shared; ROM, RAM, EPROM, EEPROM	5.7 ns	ARM architecture V5TE. This is binary backwards compatible with all previous ARM architectures.	Yes	No	Yes	Yes	Yes
BOPS		User Configurable VLIW/ PE and SP 160,32 Word Width. Internal; RAM	User configurable 32/PE word width	200 MHz, 2x2 Array, 16-bit data = 0.625 ns/tap	BOPS ManArray code compatible across 1x1, 1x2, 2x2, 2x4, 4x4, 4x4x2, 4x4x4	Yes	Yes	No	Yes	Yes
Catalina	n/a	n/a	n/a	0.02 ns per tap (complex FIR implemented in frequency domain)	Pathfinder-1 is the first product in the family	n/a	n/a	n/a	No	No
Hitachi	1	Number of memory locations: 48 K; Word width (bits) 8; internal, ROM	Memory locations: 4K word width (bits):16; internal, RAM	1	SH-1,SH-2	Yes	Yes	No	Yes	No
Hitachi	1	Memory locations: 256K word width: 8; internal, Flash	Memory locations: 4K word width (bits):16; internal, RAM	1	SH-1,SH-2	Yes	Yes	No	No	No
Hitachi	1	Memory locations: 256M word width: 8; external, SDRAM	Memory locations: 8K word width (bits):16; internal, RAM	1	SH-1,SH-2	Yes	Yes	No	Yes	No
Hitachi	1	Memory locations: 256M word width: 8; external, SDRAM	Memory locations: 4K word width (bits):16; internal, RAM	1	SH-1,SH-2	Yes	Yes	No	Yes	Yes
Hitachi	1	Memory locations: 488M word width: 8; internal & external, SDRAM	Memory locations: 8K word width (bits):16; internal, RAM	1	SH-1,SH-2, SH-3 and SH-DSP	Yes	Yes	No	Yes	No
Hitachi	1	Memory locations: 8K word width: 8; internal and external, CACHE	Memory locations: 16K word width (bits):8; internal, CACHE	1	SH-1,SH-2	Yes	Yes	No	Yes	No
Hitachi	1	Memory locations: 8K word width: 8; internal and external, CACHE	Memory locations: 16K word width (bits):8; internal, CACHE	1	SH-1,SH-2	Yes	Yes	No	Yes	Yes
Infineon	8	Memory locations: 16K word width: 24; internal and external; ROM, RAM, EPROM, EEPROM	Memory locations: 64M word width (bits):16; internal and external; ROM, RAM, EPROM	3 ns	No	Yes	Yes	Yes	Yes	No
Infineon	3	Memory locations: 16K word width: 24; internal; ROM, RAM	Memory locations: 8K word width (bits):64; internal; RAM	5 ns	n/a	Yes	Yes	Yes	Yes	Yes

Company	No. of Gen't purpose calculation units	Program Memory	Data Memory	Min. Single -Tap FIR Filter Cycle Time	Upward Code Compatible w/ What Other Part Family	C Compiler Available	Assembly Language Optimizations Tools Available	Architectural Support for C Stack Frames	JTAG Support for Emulation	Full JTAG Test Support
LSI Logic		Memory locations: 128K/1M word width: 16; internal, shared; ROM, RAM	Memory locations: 128K/1M word width: 16; internal, shared; ROM, RAM	Real: N/2 cycles. Therefore 2.5 ns per tap @ 200 MHz.	Assembler level compatibility across all processors.	Yes	No	No	Yes	Yes
Lucent		Memory locations: 64K word width: 16; internal and external; ROM, RAM, EPROM, EEPROM	Memory locations: 64K word width: 16; internal and external; RAM,	8.3 ns	DSP16000 via translator	No	No	No	Yes	Yes
Lucent		Memory locations: 1M word width: 16; internal and external, shared; ROM, RAM, EPROM, EEPROM	Memory locations: 16M word width: 16; internal, external, shared; RAM	Two taps can be calculated every clock cycle (due to dual-MAC architecture). A clock cycle is 6.6 ns resulting in a throughput of 1 tap/3.3 ns		Yes	No	Yes	Yes	Yes
Phillips		X data memory: up to 64 Kword (SRAM, ROM) Y data memory: up to 64 Kword (SRAM, ROM) X and Y data memory may be shared Memory is internal, external, shared; ROM, RAM	X data memory: up to 64 Kword (SRAM, ROM) Y data memory: up to 64 Kword (SRAM, ROM) X and Y data memory may be shared	Two taps per cycle @ 90 MHz		No	No	No	Yes	Yes
Phillips		X data memory: up to 4096K word (SRAM, ROM) Y data memory: up to 4096K word (SRAM, ROM) X and Y data memory may be shared Memory is internal, external, and shared; ROM, RAM	X data memory: up to 4096 Kword (SRAM, ROM) Y data memory: up to 4096 Kword (SRAM, ROM) X and Y data memory may be shared	Two taps per cycle @ 150 MHz		Yes	No	Yes	Yes	Yes
Phillips	27	Off-chip SDRAM up to 64MB, RAM	External SDRAM	7 ns	TriMedia and Nexperia DVP	Yes	Yes	Yes	No	Yes
Star*Core	4 DALUs	Core memory, so no memory included. Lucent & Motorola will add memory and peripherals to the final SOC products they release to market	Core memory, so no memory included. Lucent & Motorola will add memory and peripherals to the final SOC products they release to market			Yes	Yes	Yes	Yes	Yes
Texas Instruments	Same as #8	256 words x 16 bits, internal, shared, RAM	288 words x 16 bits, Internal RAM	33 ns		Yes	No	Yes	Yes	Yes
Texas Instruments	Same as #8	256 words x 16 bits, internal, shared, RAM		50 ns	No	Yes	No	Yes	Yes	Yes
Texas Instruments	Same as #8	Dependent on device type. Please contact vendor for details.	Dependent on device type. Please contact vendor for details.	Half a clock cycle per tap	All eight devices within the 'C6000 platform are completely object code	Yes	Yes	Yes	Yes	Yes
Texas Instruments	Same as #8	Word width: 32 bits, internal, shared, RAM		One clock cycle per tap	All C3x devices compatible with each other. Not code compatible with other DSPs	Yes	No	Yes	Yes	Yes for C33, No for C31 and C32
VLSI	1	Up to 4G x 32, internal, external, shared, ROM, RAM	Up to 4G x 16, internal, external, shared, ROM, RAM	1 cycle, 10 ns (in 0.25-µm technology)	VS_DSP1	Yes	Yes	No	No	No
VLSI	1	Up to 64k x 24, internal and external; ROM, RAM	Up to 2 x 64k x 24, Internal, External, ROM, RAM	1 cycle, 15 ns (0.35-µm technology)		Yes (from 3rd party)	Yes (from 3rd party)	No	No	Yes
ZiLOG		0-8K x (0-8K)x16, internal and external; ROM	512 x 256 x 16+256 x 16, internal, RAM	50 ns		Yes	No	No	No	No

Company	Low Cost Emulation Available	Full Featured Emulator Available	Peripherals Available	Mixed-Signal Versions Available	Part Numbers in the Family	URL for Datasheets	URL for Application Notes
3DSP	Yes	Yes	Yes	No	SP-5	http://www.3dsp.com/lit/lit-gateway.html	http://www.3dsp.com/lit/lit-gateway.html
3DSP	Yes	Yes	Yes	No	SP-3	http://www.3dsp.com/lit/lit-gateway.html	http://www.3dsp.com/lit/lit-gateway.html
AMSI	No	No	Yes	Yes	GEP02, GEP03, GEP04, GEP05, GEP10		
Analog Devices	Yes	Yes	Yes	Yes	ADSP-2101, ADSP 2103, ADSP 2104, ADSP 2105, ADSP 2109, ADSP 2111, ADSP 2115, ADSP 2161, ADSP-2162, ADSP-2163, ADSP-2164, ADSP-2171, ADSP-2173, ADSP-2181, ADSP-2183, ADSP-2184, ADSP-2184L, ADSP-2185, ADSP-2185L, ADSP-2185M, ADSP-2186, ADSP-2186L, ADSP-2186M, ADSP-2187L, ADSP-2187M, ADSP-2188M, ADSP-2189M	www.analog.com/dsp	www.analog.com/dsp
Analog Devices	Yes	Yes	Yes	No	ADSP-21020, ADSP-21060, ADSP-21062, ADSP-21061, ADSP-21061L, ADSP-21062L, ADSP-21065L, ADSP-21160M	www.analog.com/dsp	www.analog.com/dsp
ARM	Yes	Yes	Yes	Yes	ARM9E, ARM946E-S, ARM966E-S	http://www.arm.com/Pro+Peripherals/Cores/ARM9E	http://www.arm.com/Documentation/AppNotes/
BOPS	No	Yes	Yes	Yes	2010FX, 2010FL, 2010XL, 2010DL, 2020FX, 2020FL, 2020XL, 2020DL, 2040FX, 2040FL, 2040XL, 2040DL	http://www.bopsnet.com/publications.shtml	http://www.bopsnet.com/publications.shtml
Catalina	Yes	Yes	Yes	No	Path1-80	www.catalinaresearch.com	www.catalinaresearch.com
Hitachi	Yes	Yes	Yes: 4 DMA, 5 Serial ports, 3 16-timers, 1 Watch Dog timer	No	HD6437410F60	www.semiconductor.hitachi.com/superh	www.semiconductor.hitachi.com/superh
Hitachi	No	Yes	Yes: 4 DMA, 3 Serial Ports 9 16-Timers, 1 Watch Dog Timer	Yes	HD64F7065F60	www.semiconductor.hitachi.com/superh	www.semiconductor.hitachi.com/superh
Hitachi	Yes	Yes	Yes: 2 DMA, 6 Serial Ports 1 16-Timer, 1 Watch Dog Timer	No	HD6417612F60	www.semiconductor.hitachi.com/superh	www.semiconductor.hitachi.com/superh
Hitachi	Yes	Yes	Yes: 2 DMA, 3 Serial Ports 1 16-Timer, 1 Watch Dog Timer 1/100-Mbps Ethernet	No	HD6417615F60	www.semiconductor.hitachi.com/superh	www.semiconductor.hitachi.com/superh
Hitachi	Yes	Yes	Yes: 4 DMA, 3 Serial Ports 3 32-Timers, 1 Watch Dog Timer	Yes	HD6417729F133	www.semiconductor.hitachi.com/superh	www.semiconductor.hitachi.com/superh
Hitachi	Yes	Yes	Yes: 4 DMA, 2 Serial Ports 3 32-Timers, 1 Watch Dog Timer	No	HD6417750BP200	www.semiconductor.hitachi.com/superh	www.semiconductor.hitachi.com/superh
Hitachi	Yes	No	Yes: 4 DMA, 2 Serial Ports 5 32-Timers, 1 Watch Dog Timer PCI	No	HD6417750BP200	www.semiconductor.hitachi.com/superh	www.semiconductor.hitachi.com/superh
Infineon	Yes	Yes	Yes	No	CARMEL	WWW.CARMELDSP.COM	WWW.CARMELDSP.COM
Infineon	Yes	Yes	Yes	No	TC10GP	www.infineon.com/tricore	www.infineon.com/tricore

Company	Low Cost Emulation Available	Full Featured Emulator Available	Peripherals Available	Mixed-Signal Versions Available	Part Numbers in the Family	URL for Datasheets	URL for Application Notes
LSI Logic	Yes	Yes	Yes	No	LSI401Z LSI402Z Cores: ZSP400	www.zsp.com	www.zsp.com
Lucent	Yes	Yes	Yes	Yes	DSP1609, DSP1690, DSP1610, DSP1611, DSP1616, DSP1617, DSP1618, DSP1620, DSP1627, DSP1629, POMP16, DSP1695, DSP1673, DSP1643	http://www.lucent.com/micro/dsp/wiredoc.html	http://www.lucent.com/micro/dsp/wiredoc.html
Lucent	Yes	Yes	Yes	Yes	DSP16210, DSP16410, DSP16270, DSP16370,	http://www.lucent.com/micro/dsp/16000/dsp16000_doc.html	http://www.lucent.com/micro/dsp/16000/dsp16000_doc.html
Phillips		Yes	Yes	Yes			
Philips		Yes	Yes	Yes			
Philips	No	No	Yes	No	TM-1100 TM-1300	ww.trimedia.philips.com	www.trimedia.philips.com
Star*Core	Yes	Yes - Emulation, peripherals/memory & potentially mixed-signal and multi-core versions will be made available by Lucent & Motorola as they develop the final SOC products	Yes - Emulation, peripherals/memory & potentially mixed-signal and multi-core versions will be made available by Lucent & Motorola as they develop the final SOC products	Yes - Emulation, peripherals/memory & potentially mixed-signal and multi-core versions will be made available by Lucent & Motorola as they develop the final SOC products	DSP Core: SC140	www.starcore-dsp.com	www.starcore-dsp.com
Texas Instruments	Yes	Yes	Yes	Yes	TMS320LF2407, TMS320LF2406, TMS320LF2402, TMS320LC2406, TMS320LC2404, TMS320LC2402	www.ti.com/sc/dmc	www.ti.com/sc/dmc
Texas Instruments	Yes	Yes	Yes	Yes	TMS320F243, TMS320F241, TMS320F240, TMS320C242, TMS320C240	www.ti.com/sc/dmc	www.ti.com/sc/dmc
Texas Instruments	Yes	Yes	Yes	No	TMS320C6201, TMS320C6202, TMS320C6203, TMS320C6204, TMS320C6205, TMS320C6211, TMS320C6701, TMS320C6711		
Texas Instruments	Yes	Yes	Yes	No	TMS320C31, TMS320C32, TMS320C33		
VLSI	Yes	No	Yes	Yes	VS_DSP1, VS_DSP2	http://www.vlsi.fi/ip/	
VLSI	Yes	No	Yes	Yes	VS56000	http://vlsi.fi/ip/	http://vlsi.fi/ip/
ZiLOG	Yes	Yes	Yes	Yes	Z89321, Z89371, Z89323, Z89373, Z89223, Z89273	http://zillog.com/products/dspspecs.html	http://zillog.com/products/dspapp.html