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FEATURE ARTICLE

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Replacing 8051 RAM with Dallas Timekeeping RAM

Wouldn't you like to give your system an upgrade without a complete redesign? Bruce offers the DS-1644 nonvolatile timekeeping RAM and he recommends it for your 8051 applications needing nonvolatile external memory with timekeeping capabilities.

Design engineers are often faced with the challenge of designing at optimum efficiency and minimal cost. Sometimes they have to simply modify an existing system to expand its capabilities. Applications requiring extensive memory read and write cycles quickly rule out the possibility of using EEPROM. Other design considerations such as environmental conditions or the need for frequent replacement of batteries may rule out an external battery backup for SRAM as well.

In an attempt to provide the industry with a nonvolatile RAM solution, Dallas Semiconductor combined an intelligent CMOS control circuit, a lithium energy source, and a low-power SRAM in an encapsulated package to offer a high-density nonvolatile memory device with timekeeping and power-fail write protection.

I like using the DS1644 in 8051 applications requiring nonvolatile external memory with timekeeping abilities. Packaged in a 28-pin encapsulated DIP, or DS1644P 34-pin low pro-file powercap module board, this memory device packs a lot of bang for the buck.

A LOOK INSIDE

The DS1644 is a drop-in replacement for standard JEDEC 32K × 8 SRAM but with a few extra goodies. It contains an integrated nonvolatile SRAM, real-time clock, crystal (for the internal clock), power-fail detection circuit, and lithium energy source all in the DIP package. It can also double as a replacement for ROM, EPROM, and EEPROM as shown in Figure 1.

The internal power circuit is designed to detect low supply voltage, which Dallas refers to as Vpf or power-fail point. When V_{CC} falls below 4.5 (maximum) or 4.0 V (minimum), the internal power circuit write protects or blocks access to the internal clock registers and RAM while keeping the internal clock oscillator running.

As long as V_{CC} remains above 4.5 V, the internal RAM is accessed just like standard SRAM. Read and write access to the clock registers is gained using the control register located at 7FF8H. Figure 2 shows the internal clock register structure and control register.

The DS1644 is shipped with the internal clock oscillator turned off so the expected life begins when the clock oscillator is first turned on.

According to Dallas, in the absence

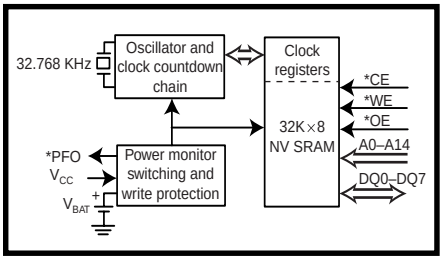

Figure 1—*Inside the encapsulated package you can see the internal setup that makes the DS1644 such a workhorse. Notice the lithium energy cell, power monitoring circuit, clock/RAM registers, and the clock/oscillator setup.*

Address	Data								Function	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
7FFF	–	–	–	–	–	–	–	–	Year	00–99
7FFE	X	X	X	–	–	–	–	–	Month	01–12
7FFD	X	X	–	–	–	–	–	–	Date	01–31
7FFC	X	FT	X	X	X	–	–	–	Day	01–07
7FFB	X	X	–	–	–	–	–	–	Hour	00–23
7FFA	X	–	–	–	–	–	–	–	Minutes	00–59
7FF9	*OSC	–	–	–	–	–	–	–	Seconds	00–59
7FF8	W	R	X	X	X	X	X	X	Control	A

*OSC = Stop bit R = Read bit FT = Frequency test
W = Write bit X = Unused

Figure 2—*Bits indicated by an X serve no function and may be used as normal RAM. The clock register data is stored in BCD format and the control register is used to gain access to the clock registers. Occupying only 8 bytes of upper RAM space leaves plenty of room for data storage.*

of V_{CC}, the internal battery lasts for ten years with the internal clock oscillator running. With V_{CC} present, the internal power source should last considerably longer because no internal energy is consumed in the presence of V_{CC} above the Vpf or V_{CC} greater than 4.5 V.

CLOCK OPERATION

The clock registers reside at the top eight RAM locations 7FF8–7FFF and are accessed using the control register, as shown in Figure 1. Most designers will appreciate this approach because it requires no programming wizardry or additional circuitry to gain access to date and time information.

Date and time information is stored in BCD format for the year, month, date, day, hours, minutes, and seconds. The internal clock register structure is double-buffered to prevent reading incorrect data during clock update cycles.

Setting bit 6 at location 7FF8 to a logic 1 (the Read bit) halts updates to the internal clock registers and enables the program to read the date and time information. Clock accuracy is guaranteed to be within ±1 min./mo. at 25° C.

DATE/TIME REGISTERS

Accessing the internal clock registers is simple and straightforward. Listing 1 is a sample of 8051 assembly code to demonstrate clock-access methods.

To begin using the clock functions, call subroutine START_OSC to fire up the internal oscillator and start the clock ticking.

Calling subroutine STOP_OSC can be used to increase the shelf life and minimize current drain on the internal lithium battery. However, stopping the internal oscillator cancels clock register updates. This option is useful if you need to remove the device from the application circuit for storage.

POWERCAP MODULE BOARD

For applications requiring a low-profile version of the DS1644, Dallas offers the DS1644P powercap module board that mates with the DS9034PCX (powercap). The DS1644P is a surface-mount package that connects directly to the powercap containing the battery and crystal, as illustrated in Figure 3.

The powercap module in Figure 4 mounts on top of the DS1644P after the ’1644P is soldered in place. This setup prevents damage to the crystal and battery inside the DS9034PCX from the high temperatures during the solder reflow process of the ’1644P. The powercap is also keyed to prevent it from being attached to the top of the ’1644P in reverse order.

Although the DS1644P offers a reduced profile, with a guaranteed clock accuracy of ±1.53 min./mo. at 25° C, its accuracy is slightly lower than the DS1644 DIP.

With this setup, replacing the battery would only be a matter of popping off the ’9034PCX. Of course, manufacturers can ship the ’9034PCX module unattached to preserve battery life until installation in the target system.

Listing 1—*This sample 8051-assembly code demonstrates clock access methods.*

```
;* DS1644 Clock Register Address *;
;       Define equates for RAM locations
YEAR        EQU 7FFFH   ; Year address
MONTH       EQU 7FFEH   ; Month address
DATE        EQU 7FFDH   ; Date address
DAY         EQU 7FFCH   ; Day address
HOUR        EQU 7FFBH   ; Hour address
MINUTES     EQU 7FFAH   ; Minutes address
SECONDS     EQU 7FF9H   ; Seconds address
CONTROL     EQU 7FF8H   ; Control register address

;* Open Clock Registers for Write Operation *;
OPEN_WRITE:
  MOV   A, #80H         ; Set bit 7 of control register
  MOV   DPTR, #CONTROL  ; Load dptr with control reg address
  MOVX  @DPTR, A        ; Send control information for Write operation
  RET

;* Close Clock Registers After a Read or Write Operation *;
CLOSE_RW:
  MOV   A, #00H         ; Load bits to close Read and Write
  MOV   DPTR, #CONTROL
  MOVX  @DPTR, A        ; Send control info to close clock registers
  RET

;* Open Clock Registers for Read Operation *;
OPEN_READ:
  MOV   A, #40H         ; Set bit 6 of control register
  MOV   DPTR, #CONTROL
  MOVX  @DPTR, A        ; Send control info t open clock for Read ops
  RET

;* Start Clock Oscillator *;
START_OSC:
  MOV   A, #00H         ; Clear bit 7 in seconds register
  MOV   DPTR, #SECONDS
  MOVX  @DPTR, A        ; Send bits to start oscillator
  RET

 ;* Stop Clock Oscillator *;
STOP_OSC:
  MOV   A, #80H         ; Set bit 7 in seconds register
  MOV   DPTR, #SECONDS
  MOV   @DPTR, A        ; Set bits to stop oscillator
  RET
```

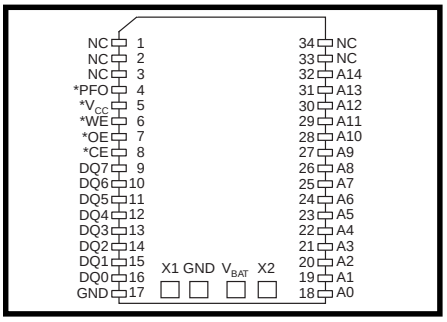

Figure 3—*For stackable controllers, or just to save space on a new design the DS1644P 34-pin low profile powercap module board offers an alternate design solution. This package fits into a standard 68-pin PLCC surface mountable socket and is functionally equivalent to the DS1644 DIP.*

DON'T NEED 32 KB?

Dallas offers a broad variety of nonvolatile SRAM solutions, from the DS1642 2K × 8 to the DS1647 512K × 8. You can directly replace EEPROM and EPROM with the Dallas nonvolatile timekeeping SRAM without any changes. This offers a powerful and cost-effective solution when it becomes necessary to upgrade existing systems.

NV SRAM VS. EEPROM

While EEPROM most certainly has its place in many design considerations, the wear-out mechanisms sometimes allow as little as 10,000 write cycles.

Suppose you use an SRAM with a 200-ns cycle time and a life expectancy of only 10,000 write cycles. The RAM would be useless in about 20 ms. Considering the cost, a serial EEPROM is a good choice for an application requiring minimal write operations and the size factor is extremely attractive for miniature applications.

DATA LOGGING

At some point, all systems designers get a little nosy, or they have a client request equipment that will log events in dismal isolated environments. In situations that require remote datalogging capabilities over extended time periods, designers will appreciate the capabilities of nonvolatile SRAM over EEPROM.

The wear-out rates of EEPROM make it a poor choice for demanding applications that require continuous or large-volume write cycles to nonvolatile storage locations. Reliability issues regarding the limited number of write cycles allowed quickly rules out EEPROM.

With no write-cycle limitations, the DS1644 can be used in intensive datalogging applications requiring large-volume read and write cycles. The ability to maintain collected data in the nonvolatile SRAM and write protect the device when V_{CC} is out of tolerance is a hard-to-resist feature.

Even an unstable power supply or power fluctuations won't corrupt the valuable data collected by a remote station. Power transitions to and from the external power source remain transparent to the internal SRAM of the DS1644.

BEEFING UP EXISTING DESIGNS

Because the DS1644 conforms, pin for pin, to the standard SRAM pinout, I can simply drop the DS1644 into an existing RAM socket on an old 8051-application board, add a small firmware upgrade, and transform it into a powerful data logger with a minimum of effort. Another application would be to use a DS1620 temperature IC to create a clock with a date, time, and temperature display.

The limited capabilities of the standard 8051 control board with external EPROM/RAM are enhanced by the addition of SRAM with battery backup, write protection, and timekeeping functions, without sacrificing I/O ports. There's no external hardware or redesign necessary, and because time is money, it's a nice option to have available.

REPLACING EPROMS

Let's explore another 8051 control board issue that's been a time-consuming burden on developers for a long time—the dreaded burn/erase cycles during the debugging phase using the old EPROM. Been there, done that, but not again.

You can use an EPROM emulator, but I can never quite keep the ribbon cable out of the way and I usually have more than enough cables and wires already cluttering my lab bench anyway. Substituting the '2764 EPROM or '2864 EEPROM with the DS1225Y 64-KB nonvolatile SRAM can eliminate the erase time.

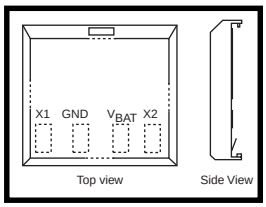

Figure 4—*The DS9034PCX powercap modules contain the lithium energy cell and clock crystal that simply snap over the top of the DS1644P.*

Many EPROM programmers program the DS1225Y the same as the '2764 so you can keep on reprogramming it without erasing it first. Need more than 8 KB? Just drop in the DS1230Y 32-KB version of the NV SRAM. Try finding a '2764 or '2864 with unlimited write cycles.

Nearly any application using standard SRAM can be enhanced with the ability to date and time stamp events or to execute certain subroutines during specific time periods. In fact, many embedded control systems would be worthless without this simple ability.

Rather than design new control systems to meet the ever-increasing demands on existing equipment, you can check out other quick and cost-effective solutions. When there's no alternative but a complete redesign of an existing control system, the engineer with the quick, cost-effective solution will probably move to the head of the class.

Bruce Reynolds works for the Colorado State Dept. of Corrections as an electronics supervisor. He also operates Reynolds Electronics, providing contract engineering services for embedded control systems, as well as building and consulting for new computer systems. You may reach him at www.rentron.com or webmaster@ rentron.com.

REFERENCE

Dallas Semiconductor, *Timekeeping and NV SRAM*, Databook, 1996.

SOURCE

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