SILICON UPDATE ONLINE

Tom Cantrell

Something Happened on the Way to the Forum

Buckle up as Tom takes a ride down the microprocessor highway and visits the Embedded Microprocessor Forum. Come to a complete stop and listen as he discusses the latest in embedded microprocessors and even gives some insight as to what kinds of products will be crossing our paths down the road.

It went embedded. That's right, the experts at MicroDesign Resources (MDR) have seen the future, and it's not just PCs and workstations.

MDR got its start many years ago when desktop CPUs were all the rage. Presided over by industry guru Mike Slater, the yearly Microprocessor Forum brings all the silicon movers and shakers together to tout their latest wonderchips and hobnob with competitors, who, in this business, are likely your next employer.

However, just last year, MDR rolled out the Embedded Microprocessor Forum. The difference with the traditional desktop forum is best indicated by the fact that this year's EMF had nary a single presentation about an '*x*86 chip.

BIG CHIPS

That's not to say that embedded chips don't have the silicon horsepower to run with desktoppers. Although they eschew massive superscalarity and speculative, out-of-order execution, the latest embedded RISCs are no slouches.

The multisourced ARM, MIPS, and PowerPC architectures dominate the high-end market. There were plenty of new chip announcements from each camp. I must confess, I haven't quite figured out how the StrongARM fits in at Intel, but that isn't stopping them from announcing a next generation due in Q1 2000.

Using the formidable Intel 0.18-µm process, the next-generation SA is expected to run at +600 MHz, while consuming a small fraction of the power (less than 0.5 W at 1.3 V for the core) of a desktop chip.

ARM announced a new ARM9E core that enhances the current ARM9 with key DSP features, such as single-cycle MAC, saturating math, and SIMD techniques (i.e., using 32-bit bandwidth to process pairs of 16-bit data). According to ARM, these relatively simple changes deliver big gains, as in 2–3 times, in signal processing performance (see Figure 1).

Freed from the shackles of SGI, MIPS has been rolling on the

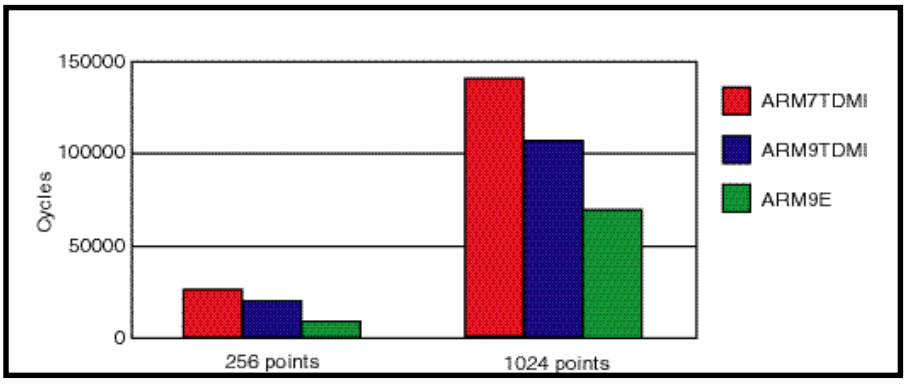

Figure 1—*When it comes to signal processing, the ARM9E proves that a little architecture enhancement goes a long way.*

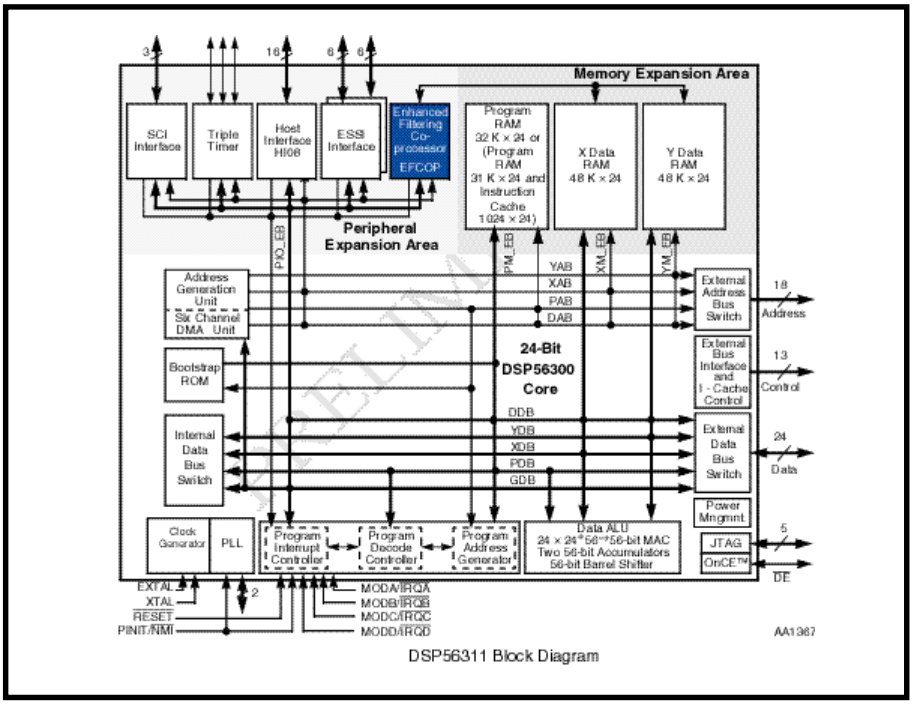

Figure 2—*Further blurring the definition of just what a DSP is or isn't, the Motorola DSP56311 incorporates a filtering coprocessor in addition to the main DSP core.*

embedded front. They announced the "new" MIPS32 architecture made up of pieces of the original, plus relatively lean and mean R3000 and R4000 designs, and DSP extensions (e.g., MAC, count leading zeroes/ones). The forthcoming Jade core, based on the new architecture, will wring a lot of performance out of a little silicon (2 mm^2) and power (1 mW/MHz).

There were other MIPS followers with announcements: QED with its high-performance copper interconnect (cuts internal R&C delays) 64-bit RM7010, Sandcraft with its 1.6-GFLOP SR1-GX, and Lexra with LX5280 (yet another DSPified RISC).

Though ARM and MIPS have dozens of supporters in their camps, the PowerPC only has two. Still, the combination of Motorola and IBM is formidable and shouldn't be underrated. While some may feel the PowerPC's fate is tied to the questionable prognosis for Apple, in fact the majority of PowerPC shipments are to non-Mac applications. Indeed, perhaps you heard the news: IBM will supply a 400-MHz PowerPC-based custom chip for Nintendo's next-generation video game.

PowerPC announcements at the Forum included a description of the so-called Book E, a joint IBM and Motorola architecture upgrade (64 bit, coprocessor interface, high-speed interrupts), and the 6.75-million transistor Motorola MPC745 and '755 with embedded enhancements such as a lockable L1 cache and dual-use L2 cache/SRAM.

DSP DEAD?

In case you haven't noticed, the distinction between DSPs and micros is blurring, as each side loots the other's quiver of architecture and tool tricks. In fact, as far as I'm concerned, the difference is more a matter of marketing than technology at this point. Processors, whatever they're called, will increasingly be called on to handle both 1s-and-0s as well as all types of signals.

In fact, I had to laugh when I got my first glimpse of the new Motorola 56311 DSP, pictured in Figure 2. Notice the little block near the top center called the Enhanced Filtering Coprocessor. It's a 24-bit filtering and echo-cancellation coprocessor that runs parallel to the DSP core. Basically, we're talking a DSP with a DSP coprocessor, highlighting the futility of trying to figure out what's a DSP and what isn't.

BENCHMARKS DEBUT

Whatever it's called or does, the only sure thing is that designers want it to go faster. The only problem is that performance is hard to predict, especially when you're sorting through the mishmash of competitive pitches and claims.

Unlike the desktop market, the embedded world has never had the luxury of SPEC or similar commercial benchmark suites. Instead, there's a motley collection of Dhrystone, VAX MIPS, and native MIP, MAC, and FLOP claims that are so vague, incomparable, and unverifiable that they border on snake oil.

Enter EEMBC (*EDN* Embedded Microprocessor Benchmark Consortium, pronounced "embassy") with the holy grail of realistic and trustworthy benchmarks for embedded applications. Under the leadership of *EDN*'s Markus Levy, EEMBC is a consortium of more than two dozen micro suppliers, including all the big names. They've come up with benchmarks for five distinct markets, including the automotive/industrial (see Table 1), consumer, networking, office automation, and telecommunications.

EEMBC faces the inevitable temptation for suppliers to optimize (er, cheat) and faces it head on with an independent certification lab and extensive rules about what's kosher

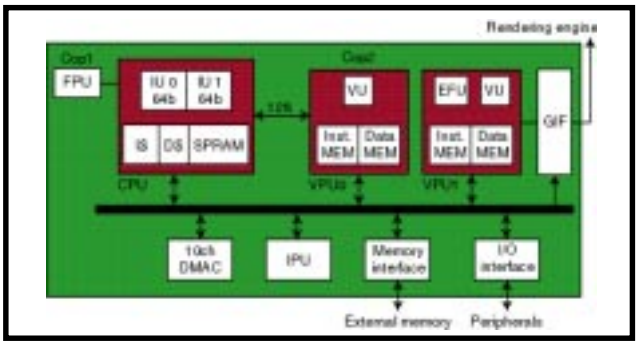

Figure 3—*Once again, video games set the price/performance standard with the Emotion Engine in the Sony Playstation 2 delivering workstation graphics performance at a Toys-R-Us price.*

	AMD K6-2 450 MHz Microsoft and Visual C/C++	ARM 920T 160 MHz ARM Development Kit 2.50	Infineon SAB C167CS 25 MHz Keil C166 Compiler V3.12	Motorola PowerPC 555 40 MHz Diab Data 4.3p, Rev. 6
Table lookup	319264.4	43478.3	1890.4	14767.0
Angle to time	715563.5	73529.4	9652.5	36273.2
PWM	1347708.9	344827.6	32679.7	59740.2
CAN	2812148.5	438596.5	45871.6	104860.8
Tooth to spark	125552.4	15151.5	761.0	4861.4
Road speed	2180444.7	454545.4	44247.8	66343.7
IIR	96374.4	9708.7	2481.4	8380.0
Bit manipulation	23738.1	3361.3	287.7	593.7
pointer chasing				
Matrix math	1375.4		3.6	65.7
Cache buster	982318.3	468750.0		
FFT	627.4	125.0	10.3	34.5
iFFT	682.7		9.1	37.2
FIR	46581.0	21276.6	1919.4	4347.8

Table 1—*Ladies and gentlemen, place your bets. EEMBC hopes their benchmarks become the standard for handicapping embedded micros.*

and what isn't, lest benchmarking end up being a programmers' contest. There'll be both out-of-the-box and optimized scores. Out-of-the-box scores give you a way to compare different C compilers for a particular chip, whereas optimized scores represent the most likely outcome for a real-world design.

EEMBC makes their living off the suppliers, not users, so the benchmark results are posted publicly on their web site at www.eembc.org.

EMOTIONAL RESPONSE

One of the highlights at the forum was a demonstration of the forthcoming Playstation 2 by Sony's VP of LSI development Hidetaka Magoshi. Though I'm not personally into Playstations, you don't have to be a video-game junkie to appreciate the technical prowess of the design. I guarantee, when you see Playstation 2 in action, it's going to blow your mind.

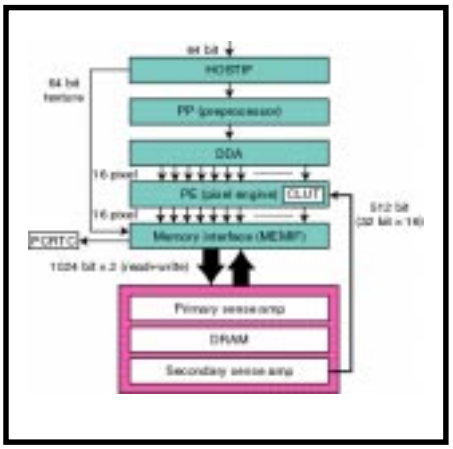

Figure 4—*The Graphics Synthesizer in the Playstation 2 proves embedded DRAM's time has come.*

Peeking under the hood reveals the secret: a high-performance chip set combining the Emotion Engine and the Graphics Synthesizer. The Emotion Engine, pictured in Figure 3, whose name aptly reflects its lofty ambition, might best be described as a single-chip Cray. It contains a beefy 64-bit MIPS CPU supplemented with two vector processing units with a total of ten floating-point multipliers and four dividers. Running at 300 MHz and exploiting 128-bit on-chip buses, the Emotion Engine blows through 3D graphics at a stunning pace. A floating-point matrix routine, consisting of 7 multiplies, 12 multiply-adds, and a divide takes only 7 cycles.

The image data is passed to the Graphics Synthesizer (see Figure 4), which integrates both the rendering engine and the 4-MB DRAM frame buffer using the latest embedded DRAM process. The reason for putting the DRAM on the same chip isn't to save a few bucks, but to achieve ultra-high 48-GBps bandwidth thanks to a 2560-bit (!) on-chip bus.

You may wonder how Sony could hope to make any profit selling a box with such state-of-the-art silicon for a couple of hundred bucks? In fact, Mr. Magoshi when asked about the cost of the chips happily replied, "Not my department." In other words, they won't make money on the box, but they can make a lot of money off game license fees, especially if they succeed in achieving the goal of inspiring emotional response.

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