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FEATURE ARTICLE

Rodger Hosking

VIM: A Powerful New Mezzanine

Have you ever noticed that the most popular standard mezzanine busses still fall short of meeting the needs of recently introduced DSP and RISC processors? Rodger presents Velocity Interface Mezzanine (VIM) as a viable solution to this I/O gap. Follow him as he takes us through VIM's three major elements—the streaming parallel bus, the serial interface, and the control status interface.

One of the toughest obstacles faced by designers of embedded real-time systems comes from the same new technology that fuels this fast-moving industry. Our insatiable demand for more powerful, smaller, and less expensive processors and peripherals has driven the wizards of silicon to produce generation after generation of increasingly faster devices. However, system infrastructures for connecting these devices to each other and to real world peripherals have not kept pace with the data transfer demands of these new devices. As a result, overall system performance often suffers more from bottlenecks in interconnections than from device speeds (see the "New Processors" sidebar).

Several factors have exaggerated this problem in open-architecture board-level embedded systems. The role of the backplane in these systems is shifting from its traditional task of providing a data-flow channel between boards to that of handling control, status, and initialization tasks. Even though some newer high-speed backplane technologies are emerging, the concept of arbitrating for a common bus shared across multiple boards proves limiting in the more demanding applications. As a result, alternate techniques for moving data across the backplane, such as RACEway, have grown in acceptance—notwithstanding the cost of implementation and packaging, which can be significant.

One of the most traditional methods of delivering dedicated high-speed interconnects between boards, is the mezzanine or daughterboard. Over the years, dozens of mezzanine architectures have evolved. Most of them were inspired by specific needs of a particular product or manufacturer, and therefore remained obscure company-proprietary designs. However, after years of use, refinement, definition, and numerous committee meetings, a few mezzanine designs have evolved into true industry standards. Unfortunately, the most popular standard mezzanine buses still fall far short of meeting the needs of recently introduced DSP and RISC processors

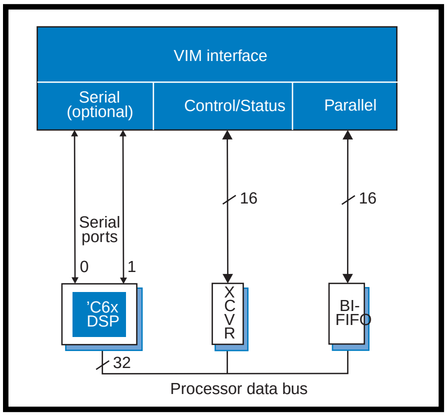

Figure 1—*The VIM Interface includes the streaming parallel bus, the serial interface, and the control/status interface.*

(see the “Comparing Mezzanine Designs” sidebar).

To close this I/O gap, Pentek developed the VIM (velocity interface mezzanine) architecture, a high-performance mezzanine bus delivering high-speed data transfers suitable for a variety of processors and board formats.

Signal	Lines	Direction	Description
Data bits	32	In/Out	Bidirectional data lines
FIFO clock	1	Out	Clock for mezzanine FIFO port
FIFO chip select	1	Out	Enables the FIFO clock for reads/writes
FIFO direction	1	Out	Determines FIFO read/write mode
FIFO input flags	3	In	Full, almost full, and almost empty
FIFO output flags	3	In	Empty, almost empty, and almost full
FIFO reset	1	Out	Clears contents of FIFO
Processor	1	In	Interrupt signal from processor
Mailbox interrupt	1	In	Interrupt from FIFO mailbox
Mailbox select	1	Out	Enables reads/writes to FIFO mailbox

Table 1—*All signals associated with the streaming parallel bus are single-ended and TTL-compatible.*

DESIGN RATIONALE

VIM was originally inspired by the need to meet the high-speed I/O demands of the Texas Instruments TSM320C6201 on Pentek’s quad processor VMEbus board, Model 4290. Although PMC modules were considered, they were soon discarded for two serious shortcomings. The maximum PMC transfer rate of 33 MHz was too low to meet the needs of many targeted peripherals like FPDP (front panel data port) and RACEway. Secondly, only two PMC sites can be accommodated on a standard 6U VME board, forcing two DSPs to share one PMC site.

We needed a mezzanine structure that could provide a private, parallel data path to each processor supporting up to 100-MHz transfer rates for 32-bit words. This is consistent with the synchronous bus cycle mode of the ’C6201 and a realistic upper limit for connector technology. We also wanted to accommodate high-speed serial interconnects for the many digital telecom interfaces and other serial peripherals. Here, maximum bit rates of up to 100 Mbps would serve the needs of most serial devices.

Lastly, a control-and-status interface was required to configure and monitor circuitry on the mezzanine card. Interrupt support was essential to minimize processor overhead and to take advantage of DMA engines found on many processors.

Mechanically, the electrical interconnection scheme needed to be small, robust, reliable, and reasonable in cost. The mezzanine card itself required sufficient real estate for circuitry and provisions for power supplies and cooling. Front panel access for the many different types of signal interfaces and the wide variety of associated connectors was essential. Provisions for shielding of critical analog and RF circuitry was mandatory to support wideband data converters and software radio functions.

Perhaps most important, we wanted a mezzanine structure that either already was an open industry standard or could evolve into one. Because no existing mezzanine standard could meet our requirements, we embarked on a new mezzanine design. To help ensure acceptance from a broad industry base, the mezzanine architecture had to be non-proprietary, royalty-free, and completely independent of any one processor or manufacturer.

OVERVIEW

While defining the new mezzanine, we focused on two parallel (and often conflicting) goals. The immediate goal was to meet the performance needs of the Models 4290 and 4291 quad ’C6x processor boards with tight development and delivery schedules. The second goal was to make decisions in implementation that would allow VIM to work not only with next-generation TI processors but also with the hottest new DSP and RISC devices from other manufacturers as well, remaining consistent with our open standard mandate.

Shown in Figure 1, the essential elements of the VIM electrical bus consist of three interfaces—the streaming parallel bus, the serial interface, and the control/status interface.

VIM STREAMING PARALLEL BUS

It became immediately apparent that we had to decouple the high-speed 32-bit streaming parallel interface from the processor. The incredibly tight timing constraints of the synchronous DRAM interface of the ’C6201 were clearly much too burdensome to impose on any open-standard bus. The asynchronous interface was much too slow. The obvious win-win solution to this problem became synchronous, bidirectional FIFO memories, or synch bi-FIFOs.

Synch bi-FIFOs provide consistent industry-standard timing and have the added benefit of buffering input and output data to the processor, taking optimal advantage of the efficient block transfers. DMA controllers supporting the processor can easily utilize the software-configurable interrupt flags of the bi-FIFOs for automatic data transfers between the processor memory and

Signal	Lines	Direction	Description
Receive data	2	Out	One line for each of two serial ports
Receive clock	2	In/Out	One line for each of two serial ports
Receive frame sync	2	Out	One line for each of two serial ports
Transmit data	2	In	One line for each of two serial ports
Transmit clock	2	In/Out	One line for each of two serial ports
Transmit frame sync	2	Out	One line for each of two serial ports
External clock	2	Out	One line for each of two serial ports

Table 2—*Signals associated with the serial ports provide a flexible and configurable interface to many serial devices.*

Signal	Lines	Direction	Description
Data bus	32	In/Out	Bidirectional data bus (buffered to processor)
Address bus	16	In	Address lines (subset of processor address)
Output enable	1	In	Enables the module to drive data bus
Read strobe	1	In	Read control signal
Write enable	1	In	Write control signal
Ready output	1	Out	Data transfer complete acknowledge
Reset	1	In	Resets or initializes the module
Clock input	1	In	Processor related clock
Interrupt output	1	Out	Interrupt to the processor
Module present output	1	Out	Indicates that a module is installed

Table 3—*Signals present on the control/status interface allow registers and other programmable module resources to be mapped into the processor memory space.*

peripheral devices, thus freeing the processor core to concentrate on more worthy tasks. Any idiosyncratic timing provisions between the processor and the bi-FIFO are transparent to the mezzanine interface. Because many processors already support synchronous DRAM interfaces, synchronous FIFOs are typically not difficult to handle.

The benefits of using bi-FIFOs for the parallel interface are numerous. With two independent ports, the bi-FIFO supports wide disparities between mezzanine data rates and processor data rates. The mezzanine port can be clocked at any rate up to its maximum of 100 MHz, supporting both fast and slow peripherals as well as clocking, which is periodic, nonperiodic, or “bursty.” Without the bi-FIFO, the processor would have to try to be ready to take or deliver data at just the right time, imposing a serious constraint on processing tasks.

On the processor side, the bi-FIFO can be loaded or unloaded whenever it is convenient, usually at the end of a processing loop when block transfers of data make the most sense. Prudent real-time signal processing design techniques require the processor task execution time for a block of data to be (at least slightly) shorter than the time it takes to collect that block. In this way, the processor finishes all of its “homework” and waits (perhaps briefly) for the next data block to become ready. Bi-FIFO buffering embodies the ideal implementation of this approach.

Bi-FIFOs also allow slower processors to handle high-speed streams. A good example is the new RACE++ standard from Mercury, which specifies 32-bit words transferred at 66.66 MHz. The 100-MHz bi-FIFO VIM port easily absorbs inbound RACEway packets and allows a slower processor to subsequently unload the data at a slower rate. Likewise, the slower processor can leisurely fill the bi-FIFO with an outgoing packet and then initiate the RACEway interface to deliver the packet at the full rate from the VIM port.

Signal	No. Pins	Total Current
+5V	20	3 A
+12 V	1	1 A
–12 V	1	1 A
GND	23	-

Table 4—*Power supply lines from the motherboard include +5 VDC and ±12 VDC; recommended maximum module dissipation is 15 W.*

NEW PROCESSORS

During the last few years, the industry has witnessed the introduction of several, incredibly fast DSP and RISC processors with remarkable benchmarks for popular algorithms and sophisticated hardware engines for caching, data movement, and addressing.

For example, Analog Devices’ new 21160 Hammerhead processor operates at a clock frequency of 100 MHz and executes six floating point instructions every 10-ns clock cycle, resulting in 600 Mflops of peak horsepower. Its 48-bit external data bus can move six bytes every 15 ns for an I/O peak transfer rate of 528 Mbps.

	TI ‘C6203	TI ‘C6701	ADI 21160	MPC750
Address bus (bits)	24	24	32	32
Data width (bits)	32 + 32	32	64	64
Bus cycle rate (MHz)	300 + 150	167	66	133
Bus rate (Mbps)	1200 + 600	667	528	1064

Table i—*Comparison of recently introduced DSP and RISC processors from Texas Instruments, Analog Devices, and Motorola.*

Even though not truly a DSP, the popular Motorola PowerPC MPC-750 (running at a 400-MHz clock rate) delivers 733 MIPS and 400 Mflops. Using its external 64-bit data bus, it can handle peak I/O rates to peripherals at over 1000 Mbps.

The recently introduced Texas Instruments TMS320C6203 DSP executes eight 32-bit instructions in parallel within a 3.33-ns instruction cycle time, yielding 2400 MIPS operation. An on-chip multiple-path ALU and four-channel DMA controller are coupled to support extremely high-speed I/O peripherals. With dual 32-bit parallel data busses, it can move data to I/O devices at a combined rate of 1800 Mbps!

Now, consider typical board-level product offerings containing four, six, or even eight of these devices on a single board. Data transfers in and out of these boards to the fast communication links (such as, RACEway, FPDP, fiber channel, and high-speed peripherals like wideband A/D converters), seriously challenging traditional I/O structures and pointing out the need for a better solution.

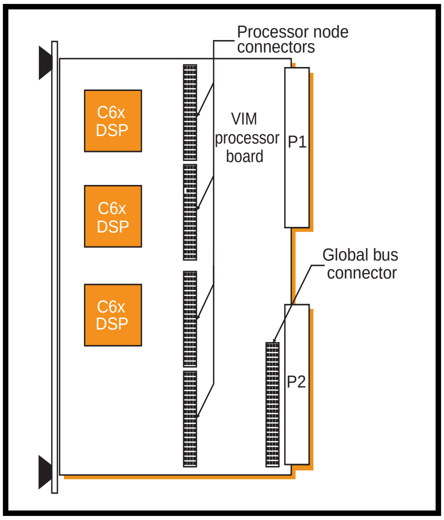

Figure 2—*On the VIM processor board, each of the four processors features its own private VIM interface which allows simultaneous full-bandwidth transfers in and out of each processor.*

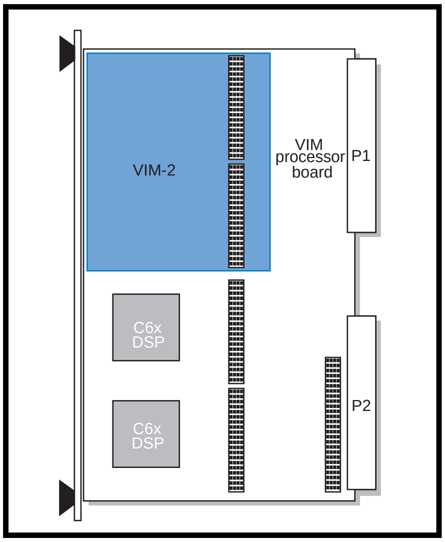

Figure 3—*The VIM-2 Module attaches to two of the four processor nodes and allows for two completely independent interfaces to each DSP.*

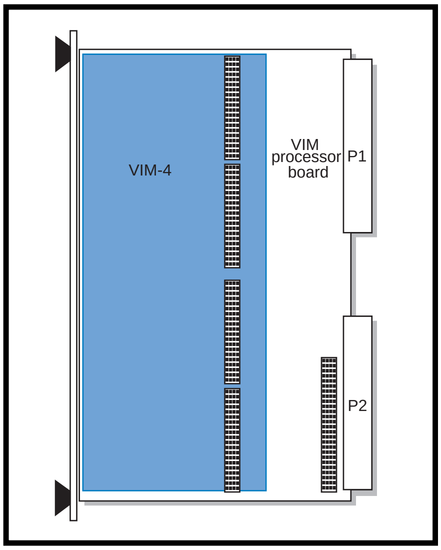

Figure 4—*The VIM-4 module provides connectivity from all front-panel connectors to all four DSPs on the processor board.*

Table 1 summarizes the signals associated with the streaming parallel bus. All signals are single ended and compliant with TTL levels. Note that the in/out signal direction is relative to the mezzanine module.

In addition to connecting to the VIM module, the VIM bi-FIFO flags are available to serve as interrupt inputs to the baseboard processor. The VIM module may also interrupt the baseboard processor by writing to one of two special mailbox registers contained within the bi-FIFO.

SERIAL PORTS

The VIM serial interface supports two full-duplex channels, each with two data lines, three clock lines, and two framing signals. These seven signals provide an extremely flexible and configurable interface to many different types of serial devices. Table 2 shows each of the lines with the direction shown relative to the mezzanine module.

The receive and transmit clock lines can be configured under software to support peripherals, which must either receive or supply clocks. An external clock signal may be applied to replace the processor's serial clock timing reference.

Many of the new processors feature integral serial ports, often with sophisticated framing and TDM hardware conveniently linked to DMA controller signals. This nicely supports serial streams from digital telecom interfaces like T1/E1 and matches the processing functions of the telecom-oriented DSPs like the 'C6203 which can handle a full T1 span of V.90 modems.

RANDOM ACCESS CONTROL/ STATUS INTERFACE

Control of the interfaces and circuitry on the mezzanine module is accommodated with the VIM random access control/status bus, which closely resembles a generic microprocessor interface. This allows registers and other programmable resources on the module to be mapped into a conveniently located read/write address region of the processor memory space.

Signals present on this portion of the VIM interface are shown in Table 3. The names of most of the lines are self-explanatory, and the direction shown is with respect to the VIM module.

POWER SUPPLY

Power supply lines from the motherboard include +5 VDC and ±12 VDC for powering the module. The number of pins for each supply and the maximum current for the module are shown in Table 4. A total maximum power dissipation of 15 W is recommended.

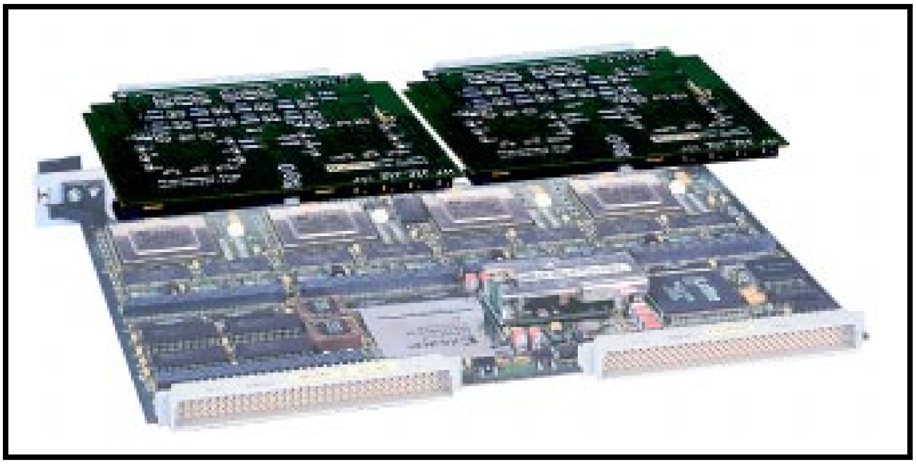

Photo 1—*VIM modules attach directly to the processor board through the I/O connectors. Shown here are two Model 6223 Comm Port Adapter VIM-2 modules in the process of being plugged into a Model 4291 Quad 'C6701 processor board, as viewed from the rear of the board. Two different modules may be used to provide more I/O functions.*

MECHANICAL ASPECTS OF VIM

Pin-and-socket-style connectors were selected for the baseboard/module interconnect. These compact 160-pin four-row connectors occupy a minimal board footprint of 2.1 × 0.25 inches and feature both male and female connectors in surface-mount versions, conserving valuable inner-layer PCB real estate.

VIM was first implemented on the Model 4290 Quad ’C6201 DSP processor, a standard 6U VMEbus board. Each of the four processors features its own private VIM interface, allowing simultaneous full-bandwidth transfers in and out of each processor. The four VIM connectors were arranged in a single line parallel to the front panel as shown in Figure 2.

A fifth connector, of the same style as the four processor VIM connectors, is installed near the rear of the board just in front of the P2 backplane connector. This 200-pin interconnect includes a shared global bus as well as the 64 user-defined pins of the VME P2 connector to support mezzanine board connections to RACEway. This fifth connector is not part of the VIM specification and can be specific to the needs of a particular baseboard.

So far, several different mezzanine module form factors have been defined for the quad ’C6x DSP boards using the VIM specification. These meet the various needs of a wide range of applications, but the first and most popular is the VIM-2 format shown in Figure 3.

The VIM-2 module has a front panel, which becomes part of the front panel of the DSP board, nesting in the same slot as the DSP board. It attaches to two of the four processor nodes and allows two completely independent interfaces to each DSP through interface circuitry to front panel I/O functions.

Photo 1 shows two VIM-2 modules being attached to the processor baseboard.

Photo 2 shows the final assembly

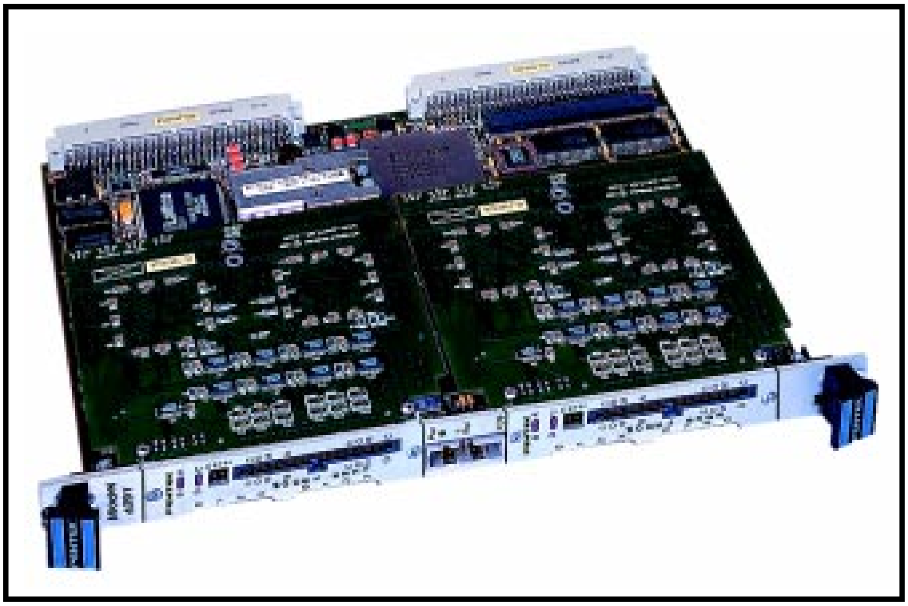

Photo 2—*The two VIM-2 modules are now fully inserted into the I/O connectors of the Model 4291 Quad ’C6701 processor board. Shown here is the completed assembly as viewed from the front. The front panels of the two modules have become part of the front panel of the 4291 processor board.*

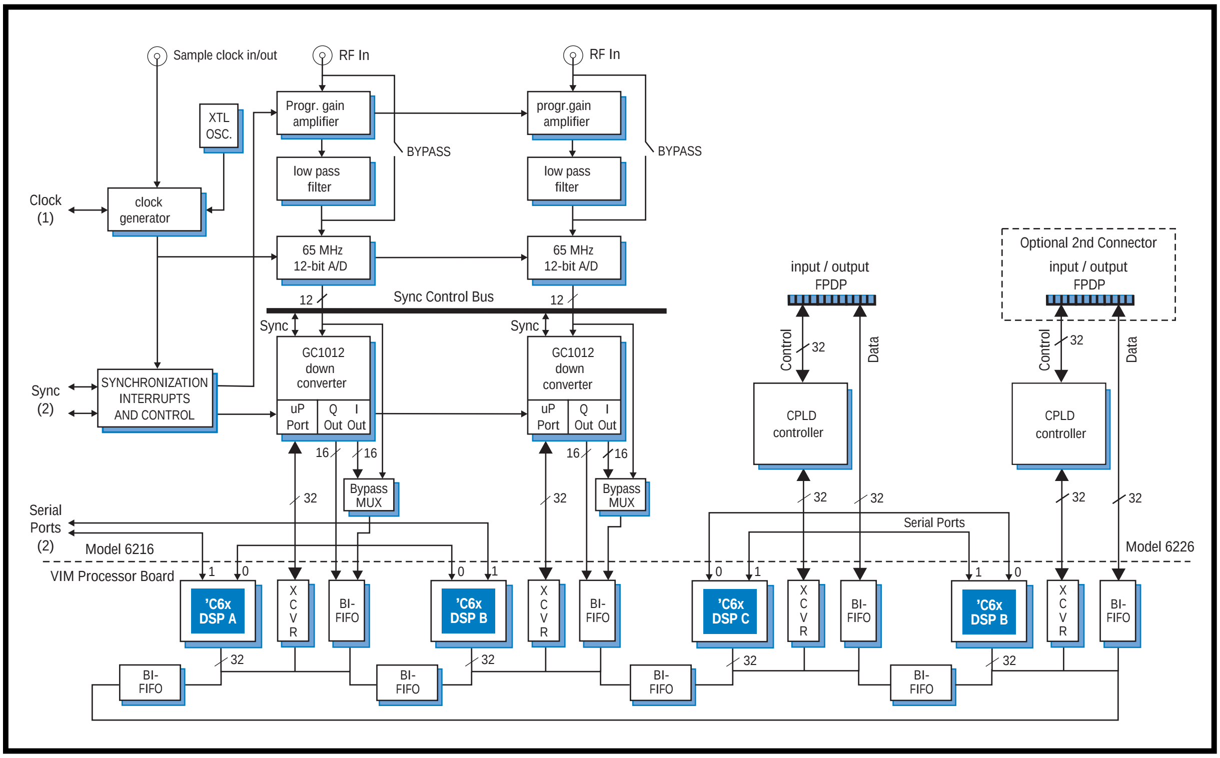

Figure 5—This single-slot VIM system shows the connections of two VIM modules to the processor board: a Model 6216 dual-channel wideband digital receiver and a Model 6226 dual FPDP module which supports 160 Mbps data transfers to other high-speed system components using an industry-standard interface.

COMPARING MEZZANINE DESIGNS

Several, popular mezzanine standards have emerged to support the configurability required by designers of COTS systems. Each mezzanine succeeded because it met specific targets in cost, size, and performance.

INDUSTRY PACK

Industry Pack is a small, low-cost module widely used for various I/O functions on standard backplane boards of nearly every type, with four IP modules fitting on a standard 6U VME board. One of its two 50-pin connectors is used for module-specific I/O to the motherboard and then often out to front-panel connectors. The second connector provides a digital interface, supporting 16-bit transfers at rates of 4 MHz on a basic, single-width module.

Double-width modules are available to double the data bus to 32 bits and provide more space for circuitry. The digital interface also includes support for two DMA channels and two interrupts. Industry Packs are cost-effective for simple, low-bandwidth I/O functions and are available from a variety of vendors.

MIX BUS

The MIX mezzanine bus was developed by Intel as a modular daughtercard standard for Multibus II systems. Pentek adopted this standard for VMEbus and offers baseboards and modules for both DSP and I/O interface functions. MIX module functions include a wide range of interfaces, including A/D and D/A converters, digital I/O functions, digital audio interfaces, SCSI controllers, digital receivers, PCM telecom transceivers, and prototyping modules. All of these functions can be combined for a nearly unlimited set of MIX subsystems handling application specific tasks.

The MIX bus includes a 32-bit data bus, 32-bit address bus, and a set of control lines, and is similar to a conventional microprocessor bus. The standard data transfer rate is 22 Mbps, but an enhanced version of the bus delivers over 40 Mbps.

PMC-PCI MEZZINE CARD

PMC has gained the attention and support of just about every board manufacturer in the high-end system-bus community, first with VMEbus vendors and now increasingly with Compact PCI vendors.

The PMC specification is a combination of two standards: the CMC (common mezzanine card) format, which defines the physical aspects, and the PCI standard, which defines the electrical interface. The physical size of the PMC module is roughly 3 × 5 inches. This size allows up to two modules to be attached to 6U VMEbus and Compact PCI boards. The module is attached to the carrier board using two, three, or four 64-pin compact connectors, depending on the application.

In addition to the four interboard connectors, the PMC specification allows for direct connection through the front panel of the VME board. A separate PMC front panel can protrude flush with the VME front panel through a cutout hole to accommodate any specialized I/O connectors required by the module. Most PMC modules utilize the 32-bit interface and are capable of moving data in block transfers at 132 Mbps.

VIM—VELOCITY INTERFACE MEZZANINE

Originally developed for Pentek's VME quad 'C6x processor board, VIM provides a three-fold interface between the baseboard and the mezzanine card. The streaming 32-bit parallel interface utilizes a synchronous, bidirectional FIFO on the baseboard, capable of operating at up to 100 MHz. The synchronous serial interface supports two 100-Mbps full-duplex channels. The control/status interface provides microprocessor-like access for reading and writing to memory-mapped registers on the mezzanine for configuring and controlling module functions.

VIM uses a high-density pin and socket connector system, which delivers these three interfaces plus power using 160 contacts. Up to four VIM interfaces fit in a single 6U VME or Compact PCI board. VIM modules feature a front panel, which replaces a section of the front panel of the baseboard to accommodate application-specific connector types for a wide range of analog and digital interfaces.

In Table i, note that the major advantage with VIM is the high I/O bandwidth per board. PMC baseboards support a maximum of two PMC modules, usually with 32-bit interfaces and a single, shared PCI bus. VIM baseboards support four dedicated, independent VIM interfaces, each capable of up to 400 Mbps.

	Industry pack	MIX	PMC	VIM
Data bus width	16 bits	32 bits	32/64 bits	32 bits
Bus cycle time	250 ns	100 ns	30 ns	10 ns
Bus cycle rate	4 MHz	10 MHz	33 MHz	100 MHz
Bus I/O BW (Mbps)	8	40	132/264	400
Buses per VME slot	4	1	1 or 2	4
I/O BW per slot (Mbps)	32	40	132/264	1600

Table i—*Comparison of bus characteristics: Industry Pack, MIX, PMC, and VIM.*

with two VIM-2 modules attached to the baseboard. Note that the complete assembly occupies only one VMEbus slot!

The VIM-2 format is especially useful because it allows two different types of VIM interfaces to be combined on the same DSP board, perhaps supporting an input function with one module and an output function with the other. Other VIM form factors include the VIM-4, which provides connectivity from all front-panel connectors to all four DSPs as shown in Figure 4.

SINGLE SLOT VIM-BASED SYSTEMS

Currently available VIM module functions include: FPDP, RACEway, digital receivers, parallel TTL I/O, serial I/O, multi-channel A/D, and high-speed A/D converters. Each module takes advantage of the high-speed parallel or serial interfaces provided by VIM, whichever is most appropriate for the module circuitry.

The example system in Figure 5 shows the Model 4290 Quad ’C6201 DSP processor VIM baseboard equipped with two VIM-2 modules. The first is the Model 6216 dual-channel wideband digital receiver, which digitizes two HF or IF band analog signals, performs a digital frequency translation, and finally delivers a baseband signal with Nyquist bandwidths from 1–32.5 MHz. Two 32-bit complex digital wideband signals are fed directly across the VIM interface into the synchronous bi-FIFOs on the processor baseboard, and subsequently, into two ’C6201s (A and B) for processing. The combined data rate for both channels is 260 Mbps.

Interprocessor bi-FIFOs (identical to the VIM bi-FIFOs) allow processors A and B to transfer data at a combined rate of up to 800 Mbps to processors C and D for more signal processing. Processors C and D finally deliver output data to a Model 6226 dual FPDP (front panel data port) VIM-2 module. Dual FPDP ports on the front panel support two 160 Mbps channels to other high-speed system components using an industry standard interface. It is important to realize that the entire system shown occupies only a single 6U VMEbus slot!

VIM SPECIFICATION

The VIM specification has been evolving for slightly more than a year now, and has been used to design custom, high-performance interfaces for complex or proprietary functions not available as standard COTS products. The benefit of being able to take advantage of the quad ’C6x processor architecture and all the supporting hardware and software tools available for it offers a significant reduction in development effort and time to market for unique or unusual applications.

Rodger H. Hosking is vice president of Pentek and was one of the founders of the company in 1986. With over 27 years experience in the electronics industry, he previously held the position of engineering manager at Rockland Systems and its successor company Wavetek Rockland. While there, he was responsible for the development of digital frequency synthesizers, FFT spectrum analyzers, and digital filter products. He designed the first commercial direct digital frequency synthesizer in 1971 and holds patents in frequency synthesis and FFT spectrum analysis techniques. Rodger has a BS degree in Physics from Allegheny College and a BS in EE and MS in EE from Columbia University.

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